

# Laser Diode Driver with APC Amplifier for Printers

## ISL58113

The ISL58113 is a high-performance laser driver that provides controlled current to grounded laser diodes. A bias current is summed with the switched current at the IOUT output, allowing the user to optimize laser diode performance.

Output switched current flows when the LVDS signal DATA is high. The output current returns to the fixed-threshold value when DATA is low. Complete I<sub>OUT</sub> shut-off is achieved by holding the CHPEN low, which will override all other control pins.

A fast settling APC amplifier connects directly to the monitor diode. The ISL58113 does not exhibit any time-dependent droop since the calibration gain is stored as a digital number.

## Ordering Information

| PART NUMBER<br>(Notes 1, 2) | PART MARKING | PACKAGE TAPE & REEL<br>(Pb-free) | PKG. DWG. # |
|-----------------------------|--------------|----------------------------------|-------------|
| ISL58113CRZ-T13             | 58113 CRZ    | 24 Ld QFN                        | L24.4x5B    |

### NOTES:

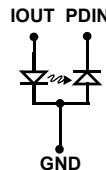
- Please refer to [TB347](#) for details on reel specifications.
- These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Features

- Voltage-controlled Output Current Source
- Very Few External Components Needed
- Internal LVDS Termination Resistors
- 200MHz Switching
- Up to 70mA Output Current
- Rise Time < 500ps
- Fall Time < 500ps
- APC Loop for Write Power Control
- Fast Settling APC Amplifier
- Single +3.3V Supply ( $\pm 10\%$ )
- Disable Feature for Power-Up Protection and Conserving Power
- Zero Droop
- Pb-Free (RoHS compliant)

## Load Configuration

- Common-cathode LD, Common-anode PD

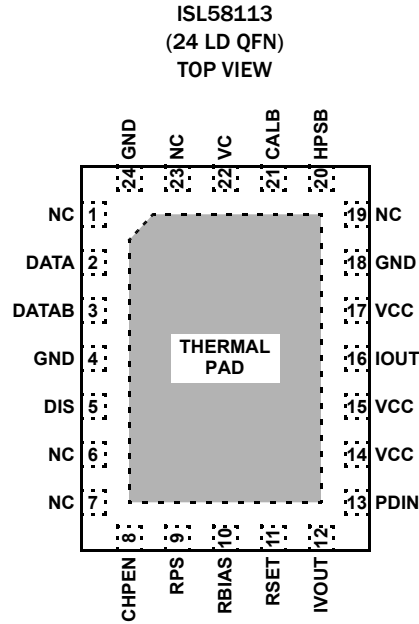


## Applications

- Laser Printer Applications
- Laser Diode Current Switching

# ISL58113

## Pin Configuration



## Pin Descriptions

| PIN NAME    | PIN NUMBER      | I/O | TYPE       | DESCRIPTION  |
|-------------|-----------------|-----|------------|--|
| DATA        | 2               | I   | LVDS       | Input data to control Laser Switching Control  |
| DATAB       | 3               | I   | LVDS       | Input data to control Laser Switching Control  |
| GND         | 4, 18, 24       |     | Ground     | Ground   |
| DIS         | 5               | I   | Digital    | Disable output current   |
| NC          | 1, 6, 7, 19, 23 | I   | No connect | No connect   |
| CHPEN       | 8               | I   | Digital    | Chip Enable; Pull High to Enable   |
| RPS         | 9               | I   | Analog     | External resistor sets the Hsync detection power   |
| RBIAS       | 10              |     | Analog     | Resistors set bias threshold current. See "Applications Information" on page 7 for more details  |
| RSET        | 11              | O   | Analog     | Bandgap derived internal reference   |
| IVOUT       | 12              | O   | Analog     | Calibrate channel with an external trimpot to GND<br>Adjust the IV amplifier gain  |
| PDIN        | 13              | I   | Analog     | Photo Diode input to the IV amplifier  |
| VCC         | 14, 15, 17      |     | Power      | Supply Voltage   |
| IOOUT       | 16              | O   | Analog     | Laser Current Output   |
| HPSB        | 20              | I   | TLL        | Hsync Power Select Enable; Active Low. During HPSB is low <u>AND</u> Hsync signal from photo detector is low, the output current is set by RPS |
| CALB        | 21              | I   | TTL        | Samples the laser power for APC; Active Low  |
| VC          | 22              | I   | Analog     | Voltage Controlling Laser Switching Current; 0V to 2V input for 0% to 100% output  |
| Thermal Pad | -               |     |            | Exposed Thermal Pad should be soldered to GND  |

NOTE: Pins with the same name are not necessary internally connected together. LDD pins must not be used for connecting together external components or features.

# ISL58113

## Absolute Maximum Ratings (T<sub>A</sub> = +25°C)

Voltages Applied to:

|                         |                                 |
|-------------------------|---------------------------------|
| V <sub>CC</sub>         | -0.5V to 4.0V                   |
| All Inputs              | -0.5V to V <sub>CC</sub> + 0.5V |
| I <sub>OUT</sub>        | -0.5V to V <sub>CC</sub>        |
| LVDS Max Current Inputs | 5mA                             |

ESD Rating

|  |       |
|--|-------|
| Human Body Model (Tested per JESD22-A114F)     | 3kV   |
| Charged Device Model (Tested per JESD22-C110D) | 1.5kV |
| Machine Model (Tested per JESD22-A115B)        | 200V  |
| Latch Up (Tested per JESD78B)                  | 100mA |

## Recommended Operating Conditions

|  |   |
|--|---|
| Thermal Resistance (Typical, Notes 3, 4) | θ <sub>JA</sub> (°C/W)  |
| 24 Ld QFN                                | 42  |
| Operating Ambient Temperature Range      | 0°C to +85°C  |
| Maximum Junction Temperature             | +150°C  |
| Storage Temperature Range                | -65°C to +150°C   |
| Pb-Free Reflow Profile                   | see link below  |
|  | <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a> |

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ<sub>JA</sub> is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
- For θ<sub>JC</sub>, the “case temp” location is the center of the exposed metal pad on the package underside.

**IMPORTANT NOTE:** All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T<sub>J</sub> = T<sub>C</sub> = T<sub>A</sub>

## Electrical Specifications V<sub>CC</sub> = 3.3V, DIS = Lo, T<sub>A</sub> = +25°C, R<sub>SET</sub> = 3.0kΩ, unless otherwise indicated.

| PARAMETER                | DESCRIPTION                        | CONDITIONS                                 | MIN (Note 5) | TYP | MAX (Note 5) | UNIT |
|--------------------------|------------------------------------|--|--------------|-----|--------------|------|
| V <sub>CC</sub>          | Supply Voltage                     |  | 3.0          | 3.3 | 3.6          | V    |
| I <sub>Sdis</sub>        | Supply Current (Disabled)          | DIS = SLPEN = HPSB = Hi                    |              | 0.1 | 1.0          | mA   |
| I <sub>S2</sub>          | Supply Current (Standby)           | DIS = Hi                                   |              | 17  | 22           | mA   |
| V <sub>LO</sub>          | Low Voltage Threshold              | All TTL inputs                             |              |     | 1.2          | V    |
| V <sub>HI</sub>          | High Voltage Threshold             | All TTL inputs                             | 2.8          |     |              | V    |
| I <sub>LO</sub>          | Input Low Current                  | All TTL inputs                             | -10          | -5  |              | μA   |
| I <sub>HI</sub>          | Input High Current                 | All TTL inputs                             | -1           |     | 1            | μA   |
| V <sub>SHUT</sub>        | VCC Shut Down Voltage              |  |              | 2.5 | 2.8          | V    |
| V <sub>LVDS</sub>        | LVDS Input Level                   | Differential, with V <sub>cm</sub> = 1.25V |              | 0.2 |              | V    |
| V <sub>CMR</sub>         | LVDS Common Mode Voltage Range     | 300mV <sub>p-p</sub>                       | 0.2          |     | 2.2          | V    |
| V <sub>C</sub>           | Control Voltage                    |  | 0.3          |     | 1.45         | V    |
| R <sub>Termination</sub> | Internal LVDS Termination Resistor |  |              | 180 |              | Ω    |

# ISL58113

## Laser Amplifier Output $V_{CC} = 3.3V$ , DIS = Lo, $T_A = +25^\circ C$ , $R_{SET} = 3.0k\Omega$ , unless otherwise indicated.

| PARAMETER                | DESCRIPTION                           | CONDITIONS  | MIN<br>(Note 5) | TYP | MAX<br>(Note 5) | UNIT    |
|--------------------------|---------------------------------------|---|-----------------|-----|-----------------|---------|
| <b>I<sub>OUT</sub></b>   |                                       |   |                 |     |                 |         |
| I <sub>OUTSW-max</sub>   | Switched Output Current               | VC = 1.45V  | 40              | 47  |                 | mA      |
| I <sub>OUTBIAS-max</sub> | Bias Output Current                   | R <sub>BIAS</sub> = 1k $\Omega$                           | 25              | 30  |                 | mA      |
| I <sub>OFF</sub>         | Output Off Current                    | DIS pin set to HIGH                                       | -75             | 0   | +75             | $\mu A$ |
| FREQ <sub>OP</sub>       | Operating Frequency                   | I <sub>OUT</sub> = maximum switch current                 | 200             | 275 |                 | MHz     |
| I <sub>OUTPSRR</sub>     | I <sub>OUT</sub> Supply Sensitivity   | I <sub>OUT</sub> = 20mA, V <sub>CC</sub> = 3.3V $\pm$ 10% |                 | 9   |                 | %/V     |
| t <sub>R-IOUT</sub>      | I <sub>OUT</sub> Rise Time            | 10% to 90%; typical LD for printer                        |                 | 0.5 |                 | ns      |
| t <sub>F-IOUT</sub>      | I <sub>OUT</sub> Fall Time            | 90% to 10%; typical LD for printer                        |                 | 0.7 |                 | ns      |
| OUTENx_t <sub>on</sub>   | I <sub>OUT</sub> on Propagation Delay | DATAx crossing to I <sub>OUT</sub> at 50% of final value  |                 | 5   | 7               | ns      |
| VC <sub>BW</sub>         | Bandwidth of VC                       | VC = 1.0V   |                 | 12  |                 | MHz     |

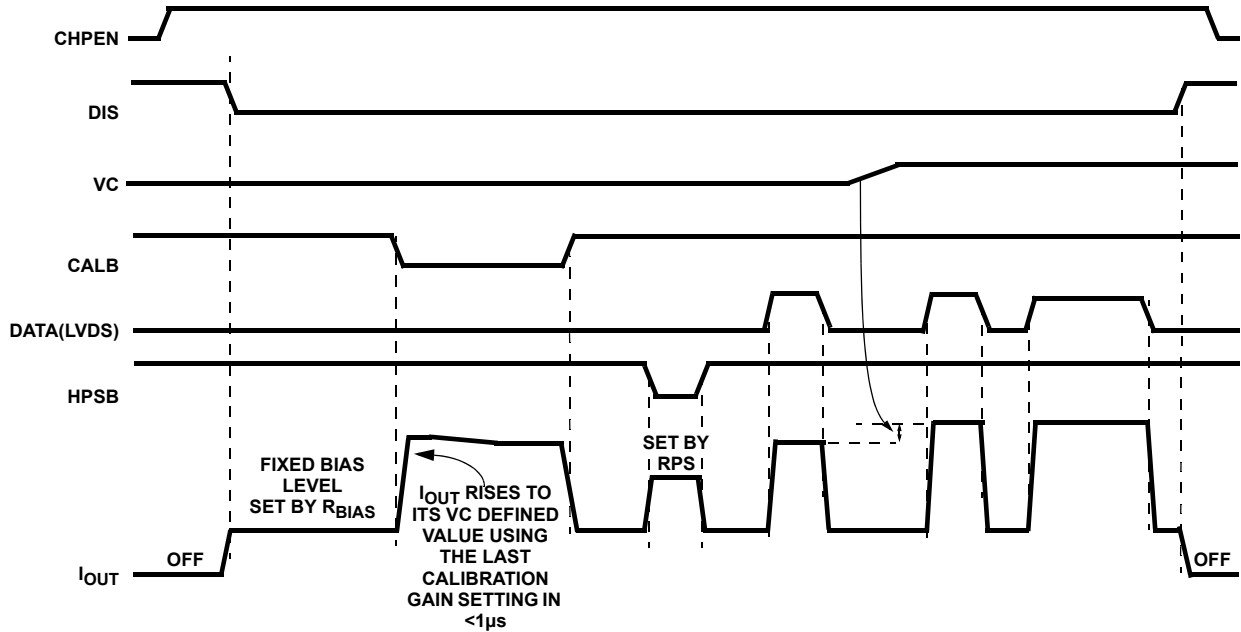
## APC Electrical Specifications $V_{CC} = 3.3V$ , DIS = Lo, $T_A = +25^\circ C$ , $R_{SET} = 3.0k\Omega$ , unless otherwise indicated.

| PARAMETER           | DESCRIPTION       | CONDITIONS                                       | MIN<br>(Note 5) | TYP | MAX<br>(Note 5) | UNIT       |
|---------------------|-------------------|--|-----------------|-----|-----------------|------------|
| t <sub>APC-50</sub> | APC Response Time | 0.3V to 1V step of VC                            |                 | 7.5 |                 | $\mu s$    |
| I <sub>V</sub> gain | IV Amplifier Gain | External resistor R <sub>IV</sub> = 500 $\Omega$ |                 | 3.1 |                 | k $\Omega$ |

### NOTE:

- Parameters with MIN and/or MAX limits are 100% tested at +25 $^\circ C$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

## Timing Diagram

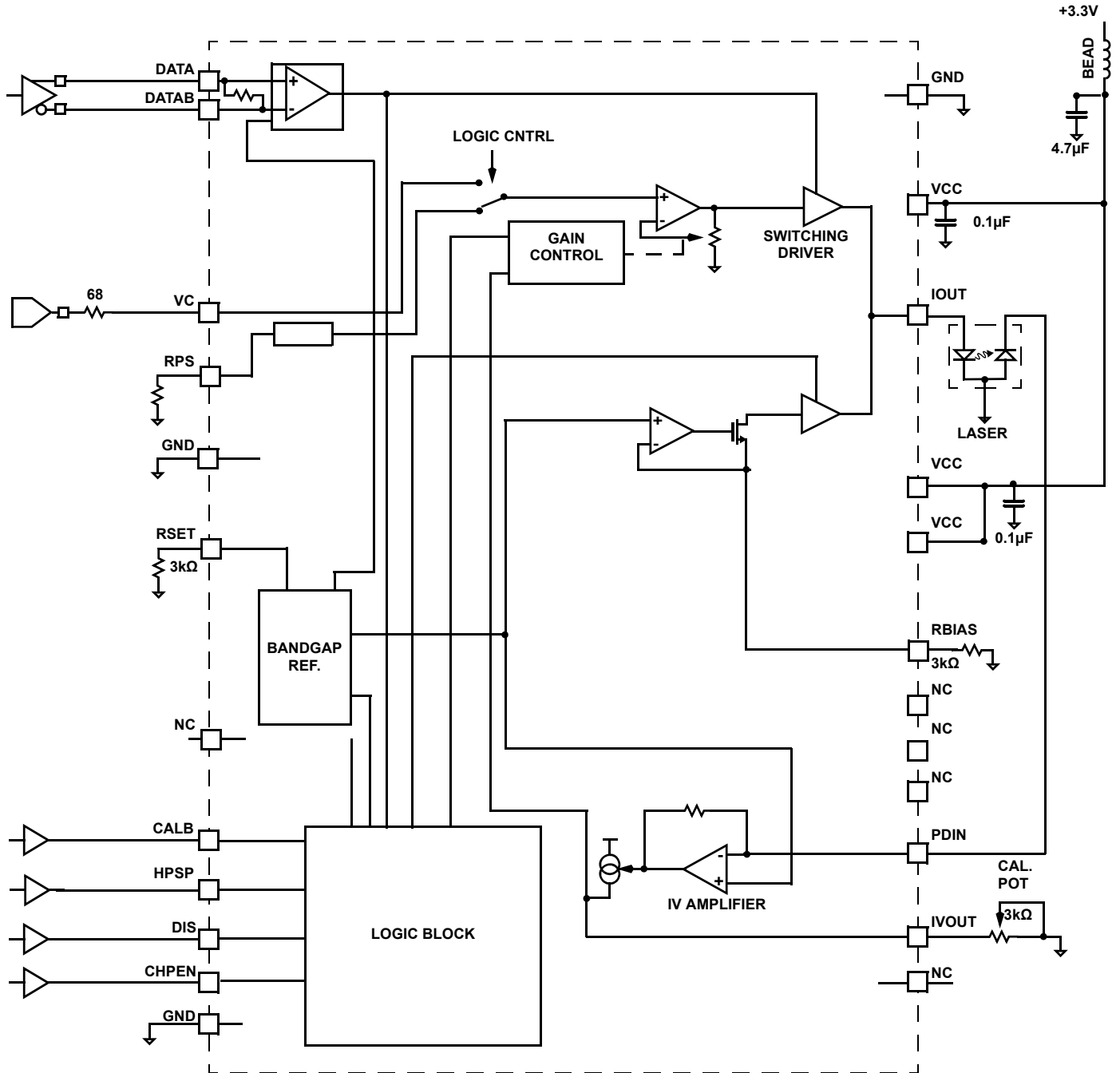


## I<sub>OUT</sub> Control

| CHPEN  | DIS | DATA | CALB | HPSB | I <sub>OUT</sub>           | COMMENTS                                  |
|--|-----|------|------|------|----------------------------|---|
| <b>POWER-DOWN (SLEEP MODE)</b>                             |     |      |      |      |                            |   |
| 0  | x   | x    | x    | x    | OFF                        | CHPEN is slow to enable                   |
| <b>STANDBY (FULL STANDBY CURRENT, NO I<sub>OUTS</sub>)</b> |     |      |      |      |                            |   |
| 1  | 1   | x    | x    | x    | OFF                        | Full standby current, no I <sub>OUT</sub> |
| <b>NORMAL DRIVE</b>  |     |      |      |      |                            |   |
| 1  | 0   | x    | 1    | 1    | ON, BIAS ONLY              |   |
| 1  | 0   | x    | 0    | 1    | ON, CAL to level set by VC |   |
| 1  | 0   | 1    | 1    | 1    | ON                         |   |
| <b>Hsync POWER</b>   |     |      |      |      |                            |   |
| 1  | 0   | x    | 1    | 0    | Hsync power                | Output current defined by RPS             |
| <b>INVALID LOGIC COMBINATION</b>                           |     |      |      |      |                            |   |
| 1  | 0   | x    | 1    | x    | INVALID                    |   |

NOTE: DATA1 and DATA2: 1 implies DATA>DATA2, 0 implies DATA<DATA2

## Typical Application



## Applications Information

### APC System Overview

As the laser heats up (or ages) its output power declines relative to the applied current, so some form of power control is required. The laser is optically coupled to a photo-diode, so that the laser's optical output can be measured. Laser optical output power is controlled by comparing the externally applied control voltage with the voltage produced by the IV-amplifier which converts the photo-diode's output current into a voltage. Since the calibrated gain is stored as a digital number in a register, the ISL58113 exhibits none of the time-dependent droop that is seen in most printers' laser diode drivers. This is of particular importance during high dot/inch graphics modes where the line may be slowed down very significantly to allow 2400 dots per inch or even more.

### Fixed-Threshold Laser Bias Control

When a laser is driven from below threshold to well above threshold, it exhibits a few cycles of a damped oscillation. The amplitude of this oscillation is minimized when the laser is kept above threshold. The "fixed" bias mode is set by asserting a logic Low on the SLPEN pin. To set the laser bias threshold currents,  $I_{BIAS}$ , connect external resistors from RBIAS pins to GND. Figure 1 shows value of  $R_{BIAS}$  corresponding to desired bias current.

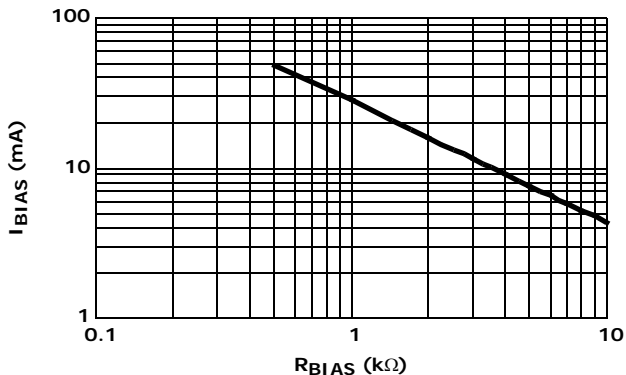


FIGURE 1.  $R_{BIAS}$  vs BIAS CURRENT

### Scaling External Resistors

$R_{SET}$  is used to scale the switching output current. Switching output current,  $I_{SW}$ , is the function of VC and  $R_{SET}$ .

$$I_{SW} = I_{SWGain} \times \left( \frac{VC}{R_{DAC}} - \frac{2}{R_{SET}} \right) \quad (EQ. 1)$$

Where  $I_{SWGain} = \sim 17$ ,  $R_{DAC} = 400\Omega$ .

$R_{BIAS}$  sets bias threshold current. Figure 1 exhibits the relationship between  $I_{BIAS}$  and  $R_{BIAS}$ . The bias current is set as Equation 2:

$$I_{BIAS} = BiasChannelGain \times \frac{InternalVref}{R_{BIAS}} \quad (EQ. 2)$$

Where  $BiasChannelGain = \sim 40$ ,  $InternalVref = 1.0V$ .

### Controlling the Sampling

The switching levels are sampled independently. This can be done during the "off-paper" period.

During calibration mode, the internal servo control will bring the laser diode output power level to match the voltage control level set by VC voltage.

### Horizontal Edge Detection

When HPSB is low, the output current is set by RPS. Asserting HPSB low overrides both channel data inputs. HPSB should not be asserted low during a calibration cycle. When HPSB is low, the desired output current  $I_{RPS}$  is governed by the following Equation:

$$I_{RPS} = 40 \times \frac{RPS}{CalDAC} \times \frac{1.05V}{RSET} \quad (EQ. 3)$$

where the CalDAC setting (from the last write power calibration) ensures laser temperature and aging compensation. The CalDAC's units are ohms. Full scale is about  $380\Omega$  and CalDAC is defined as  $CalDAC = 255/code * 380\Omega$ .

The horizontal sync pulse is meant to be a power level that overrides VC calibration and sets the output current to a fixed level.

### Typical Application

Upon the printer being powered up, the lasers should be calibrated. This would establish nominal light power outputs, typically a few milliwatts at the laser regardless of the ambient temperature and also any laser aging.

Once everything is ready for printing, the paper is in position and the mirror-motor is phase-locked then the print line(s) can be written. Before, or after, the beam is over the photo-sensitive drum, each laser can be re-calibrated. This continual re-calibration will compensate for any temperature drift of the laser, especially at the initial warming up period.

Since the calibrated gain is stored as a digital number in a register, the ISL58113 exhibits no time-dependent droop. With no droop to degrade performance the only limitation now is the lasers' own temperature change along the line. This in turn can be compensated for to some extent by adding a data-dependent compensation signal to the analog VCx input pin. It may be found that in fast draft modes for example, that the laser temperature change is sufficiently small that many lines can be written before the laser(s) need to be re-calibrated. If the printed page has a low enough duty cycle, no re-calibration may be needed at all.

The ISL58113 has analog voltage inputs to allow the laser power level to be adjusted during the line. Typically this would be driven with a PWM, low bandwidth signal to compensate for the differing beam path length as the beam is swept from one side of the page to the other.

## Note on Illegal Logic Combination

In normal use, CALB going low (active) without DIS being low (active) would be meaningless. Likewise with HPSB going low (active). Therefore, a combination of these should be avoided at all times. If this combination is applied, the chip will not work properly. To exit this mode, either set CALB to Low or/and DIS to Hi.

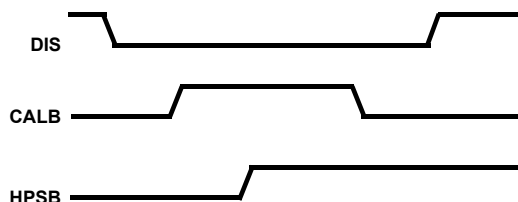


FIGURE 2. ILLEGAL COMBINATION

## Power Supply Decoupling

Due to the high values of current being switched rapidly on and off, it is important to ensure that the power supply is well decoupled to ground. During switching, the  $V_{CC}$  undergoes severe current transients, thus every effort should be made to decouple the  $V_{CC}$  as close to the package as possible. Symptoms that could arise include poor rise/fall times, current overshoot, and poor settling response. It is recommended that VCC inputs should be bypassed with  $4.7\mu\text{F} // 100\text{nF} // 470\text{pF}$  to GND.

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

| DATE    | REVISION | CHANGE                               |
|---------|----------|--------------------------------------|
| 7/29/13 | FN7659.1 | Conversion to new Intersil Template. |
| 6/23/10 | FN7659.0 | Initial release.                     |

## About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at [www.intersil.com](http://www.intersil.com).

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at [www.intersil.com](http://www.intersil.com). You may report errors or suggestions for improving this datasheet by visiting [www.intersil.com/en/support/ask-an-expert.html](http://www.intersil.com/en/support/ask-an-expert.html). Reliability reports are also available from our website at <http://www.intersil.com/en/support/qualandreliability.html#reliability>

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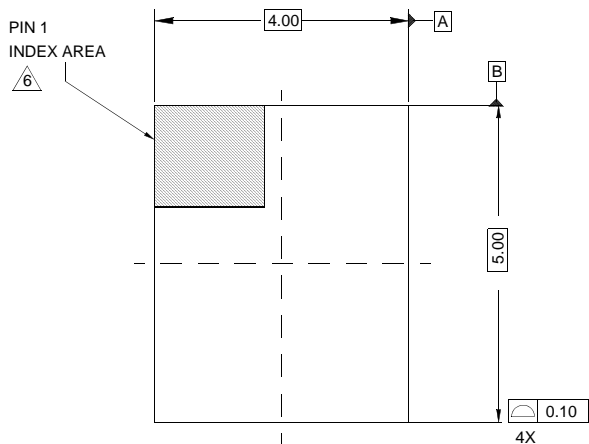


## Package Outline Drawing

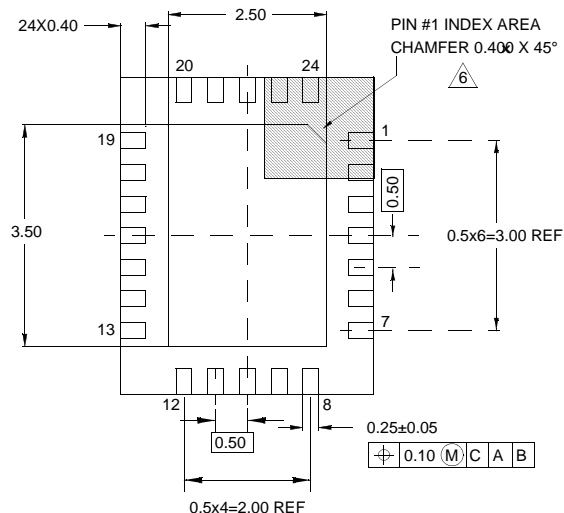
### L24.4x5B

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

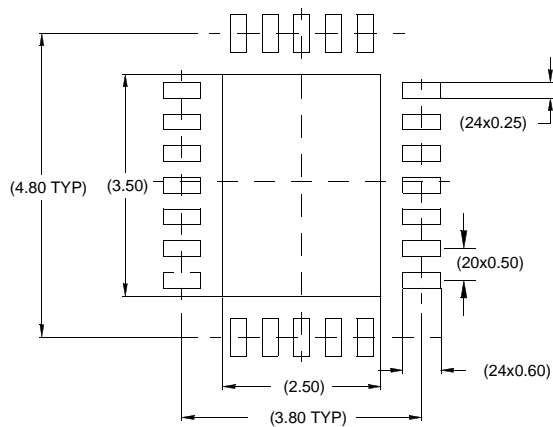
Rev 0, 10/06



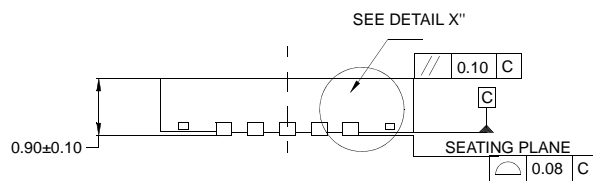
TOP VIEW



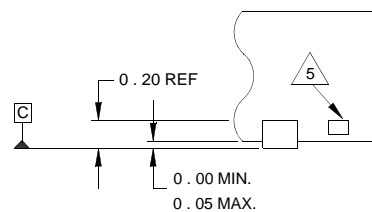
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

#### NOTES:

- Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
- Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
- Unless otherwise specified, tolerance : Decimal ± 0.05
- Dimension b applies to the metallized terminal and is measured between 0.20mm and 0.30mm from the terminal tip.
- Tiebar shown (if present) is a non-functional feature.
- The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.